We Claim:

1. A solid-state memory system comprising:

an array of memory cells, each cell capable of having its threshold voltage programmed or erased to an intended level within a range supported by the memory system;

monitoring means invoked at predefined events of the memory system for identifying any cells whose threshold voltage has shifted beyond a predetermined margin from its intended level; and

writing means for re-writing the threshold voltage of each said identified cells back to its intended level.

2. A solid-state memory system as in claim 1, wherein said predefined events of the memory system are memory operations on a portion of the memory array that are liable to perturb cells in other portions of the memory array.

3. A solid-state memory system as in claim 2, wherein said memory operations include programming operations.

4. A solid-state memory system as in claim 2, wherein said memory operations include programming and erasing operations.

5. A solid-state memory system as in claim 2, wherein said memory operations include read operations.

6. A solid-state memory system as in claim 1, wherein said predefined events of the memory system are memory operations on a portion of the memory array

that are liable to perturb cells within said portion of the memory array.

7. A solid-state memory system as in claim 6, wherein said memory operations include read operations.

8. A solid-state memory system as in claim 1, wherein:

said memory array is partitioned into a plurality of sectors, each sector having cells that are all at a time subjected to one of said specific regular memory operations; and

said monitoring means samples a predetermined number of sectors during each invocation, such that statistically each sector in the memory array gets monitored after at most a predetermined number of said predefined events.

9. A solid-state memory system as in claim 8, wherein said predefined events of the memory system are memory operations on a portion of the memory array that are liable to perturb cells in other portions of the memory array.

10. A solid-state memory system as in claim 9, wherein said memory operations include programming operations.

11. A solid-state memory system as in claim 9, wherein said memory operations include programming and erasing operations.

12. A solid-state memory system as in claim 9, wherein said memory operations include read operations.

13. A solid-state memory system as in claim 8, wherein said predefined events of the memory system are memory operations on a portion of the memory array that are liable to perturb cells within said portion of the memory array.

14. A solid-state memory system as in claim 13, wherein said memory operations include read operations.

15. In a solid-state memory system including an array of memory cells, each cell capable of having its threshold voltage programmed or erased to an intended level within a range supported by the memory system, wherein soft errors may arise from cells with a shifted threshold voltage, a method for detecting and correcting soft errors comprising the steps of:

monitoring at predefined events of the memory system to identify any cells whose threshold voltage has shifted beyond a predetermined margin from its intended level; and

re-writing the threshold voltage of each said identified cells back to its intended level.

16. A method for detecting and correcting soft errors in a solid-state memory system as in claim 15, wherein said predefined events of the memory system are memory operations on a portion of the memory array that are liable to perturb cells in other portions of the memory array.

17. A method for detecting and correcting soft errors in solid-state memory system as in claim 16, wherein said memory operations include programming operations.

18. A method for detecting and correcting soft errors in solid-state memory system as in claim 16, wherein said memory operations include programming and erasing operations.

19. A solid-state memory system as in claim 16, wherein said memory operations include read operations.

20. A solid-state memory system as in claim 15, wherein said predefined events of the memory system are memory operations on a portion of the memory array that are liable to perturb cells within said portion of the memory array.

21. A solid-state memory system as in claim 20, wherein said memory operations include read operations.

22. A method for detecting and correcting soft errors in solid-state memory system as in claim 15, wherein:

said memory array is partitioned into a plurality of sectors, each sectors having cells that are all at a time subjected to one of said specific regular memory operations; and

said monitoring means samples a predetermined number of sectors during each invocation, such that statistically each sector in the memory array gets monitored after at most a predetermined number of said predefined events.

23. A method for detecting and correcting soft errors in solid-state memory system as in claim 22, wherein said predefined events of the memory system are

memory operations on a portion of the memory array that are liable to perturb cells in other portions of the memory array.

24. A method for detecting and correcting soft errors in solid-state memory system as in claim 23, wherein said memory operations include programming operations.

25. A method for detecting and correcting soft errors in solid-state memory system as in claim 23, wherein said memory operations include programming and erasing operations.

26. A solid-state memory system as in claim 23, wherein said memory operations include read operations.

27. A solid-state memory system as in claim 22, wherein said predefined events of the memory system are memory operations on a portion of the memory array that are liable to perturb cells within said portion of the memory array.

28. A solid-state memory system as in claim 27, wherein said memory operations include read operations.

29. A solid-state memory system capable of recovering from read errors, including an array of memory cells, each cell capable of having its threshold voltage programmed or erased to an intended level within a range supported by the memory system, reading means to determine a cell's memory state by comparing the cell's threshold voltage with a read reference level, wherein through use of the memory system, read errors may be

caused by the threshold voltage of one or more cells drifted from its intended level, said solid-state memory system comprising:

error checking means associated with each of a plurality of groups of cells for identifying read errors therein;

means for adjusting the read reference level before each read operation on a group of cells containing read errors, each time the read reference level being displaced a predetermined step from a reference level for normal read, until said error checking means no longer indicates read errors; and

writing means for re-writing the drifted threshold voltage of each cell associated with a read error to its intended level.

30. A solid-state memory system capable of recovering from read errors, including an array of memory cells, each cell capable of having its threshold voltage programmed or erased to an intended level within a range supported by the memory system, reading means to determine a cell's memory state by comparing the cell's threshold voltage with a read reference level, wherein through use of the memory system, read errors may be caused by the threshold voltage of one or more cells drifted from its intended level, said solid-state memory system comprising:

error checking and correcting means associated with each of a plurality of groups of cells for identifying read errors therein and correcting a predetermined maximum number thereof;

means for adjusting the read reference level before each read operation on a group of cells containing read errors exceeding said predetermined maximum number, each time the read reference level being displaced a predetermined step from a reference level for normal

read, until said error checking and correcting means indicates read errors not exceeding said predetermined maximum number, thereby allowing said error checking and correcting means to correct the read errors; and

writing means for re-writing the drifted threshold voltage of each cell associated with a read error to its intended level.

31. A solid-state memory system capable of recovering from read errors as in claim 30, wherein said error checking and correcting means is provided by an error correction code.

32. In a solid-state memory system including an array of memory cells, each cell capable of having its threshold voltage programmed or erased to an intended level within a range supported by the memory system, wherein hard errors may arise from cells with a threshold voltage drifted sufficiently from its intended level to cause read errors, a method for recovering from said hard errors comprising the steps of:

providing an error checking scheme for each of a plurality of groups of cells for identifying read errors therein;

adjusting the read reference level before each read operation on a group of cells containing read errors, each time the read reference level being displaced a predetermined step from a reference level for normal read, until said error checking means no longer indicates read errors; and

re-writing the drifted threshold voltage of each cell associated with a read error to its intended level.

33. In a solid-state memory system including an array of memory cells, each cell capable of having

its threshold voltage programmed or erased to an intended level within a range supported by the memory system, wherein hard errors may arise from cells with a threshold voltage drifted sufficiently from its intended level to cause read errors, a method for recovering from said hard errors comprising the steps of:

providing an error checking and correcting scheme for each of a plurality of groups of cells for identifying read errors therein and correcting a predetermined maximum number thereof;

adjusting the read reference level before each read operation on a group of cells containing read errors exceeding said predetermined maximum number, each time the read reference level being displaced a predetermined step from a reference level for normal read, until said error checking and correcting means indicates read errors not exceeding said predetermined maximum number, thereby allowing said error checking and correcting means to correct the read errors; and

re-writing the drifted threshold voltage of each cell associated with a read error to its intended level.

34. A method for recovering from said hard errors in a solid-state memory system as in claim 33, wherein said error checking and correcting means is provided by an error correction code.

add A2

add B1

add C1

add D1